What Is Claimed Is:

1. A memory device comprising: a nonvolatile memory; a buffer memory having a higher access speed than the nonvolatile memory; and a control circuit,

wherein the control circuit creates a preread data management table that associates a logical address of preread data specified by a preread command inputted from the outside and a buffer memory address for storing the preread data, reads data specified by the command from the nonvolatile memory and stores the data in the buffer memory as preread data, and when a logical address specified in a read command inputted from the outside matches a logical address associated by the preread data management table, outputs corresponding preread data from the buffer memory.

2. The memory device according to claim 1,

wherein the preread command specifies preread data by a logical address.

3. The memory device according to claim 1,

wherein the preread command specifies preread data by a file name.

4. The memory device according to claim 1,

wherein the control circuit transfers preread data to the buffer memory during execution of a preread command.

5. The memory device according to claim 1,

wherein the control circuit creates a preread data management table before transferring preread data to the buffer memory.

6. The memory device according to claim 5,

wherein the control circuit transfers preread data to the buffer memory in a command wait state after the termination of execution of a preread command.

7. The memory device according to claim 1,

wherein the preread data management table includes areas for storing a start logical address of preread data, a start memory address of an area storing the preread data, and a data count of the preread data.

8. The memory device according to claim 6,

wherein the preread data management table includes an area for holding a flag indicating the validity of corresponding preread data.

9. The memory device according to claim 3,

wherein the preread data management table includes an area for holding a file name containing preread data.

10. The memory device according to claim 1,

wherein the preread data management table includes an area for holding an access count of preread data.

11. The memory device according to claim 10,

wherein, when no unused area for storing preread data is present in the buffer memory, the control circuit

searches for a buffer memory address infrequently accessed, based on an access count held in the preread data management table, and allocates an area of the located buffer memory address to a new area for storing preread data.

12. The memory device according to claim 1,

wherein the control circuit saves preread data management tables to a preread data management table save area of the nonvolatile memory in a predetermined timing.

13. The memory device according to claim 12,

wherein in response to power on, the control circuit reads a preread data management table from the nonvolatile memory, and transfers preread data located by the preread data management table from the nonvolatile memory to the buffer memory.

14. A memory device including: a nonvolatile memory; a buffer memory having a higher access speed than the nonvolatile memory; and a control circuit,

wherein, in response to a read command inputted from the outside, the control circuit consults rewritable preread data management tables that associate logical addresses of preread data and buffer memory addresses for storing the preread data, determines whether the buffer memory holds data specified by the command, if the buffer memory holds the data, outputs data read from the buffer

memory to the outside, and otherwise, outputs data read from the nonvolatile memory to the outside.

15. The memory device according to claim 14,

wherein the control circuit reads preread data management tables from the nonvolatile memory in response to power on, and transfers preread data located by the read preread data management tables from the nonvolatile memory to the buffer memory.

16. A memory device including: a nonvolatile memory; a buffer memory having a higher access speed than the nonvolatile memory; and a control circuit,

wherein in response to a preread command inputted from the outside, the control circuit creates a preread data management table that associates a logical address of preread data specified by the command and a buffer memory address for storing the preread data, and reads data specified by the command from the nonvolatile memory and stores the data in the buffer memory as preread data so that the preread data stored in the buffer memory can be outputted to the outside.

17. The memory device according to claim 16,

wherein when no unused area for storing preread data is present in the buffer memory, the control circuit allows selection between permission and inhibition of overwriting to areas already holding preread data.

18. The memory device according to claim 17,

wherein the overwrite permission is total permission for overwriting to an area already holding preread data or partial permission for overwriting to an area infrequently accessed.

19. The memory device according to claim 16,

wherein, in response to a read command inputted from the outside, the control circuit consults the preread data management table to determine whether the buffer memory holds data specified by the command, and if the buffer memory holds the data, outputs data read from the buffer memory to the outside, otherwise, outputs data read from the nonvolatile memory to the outside.

20. The memory device according to claim 16 or 19,

wherein, in response to a write command inputted from the outside, the control circuit consults the preread data management table to determine whether the buffer memory holds data of a write address specified by the command, and if the buffer memory holds the data, updates the data of the buffer memory by write data along with data of the nonvolatile memory, otherwise, updates data of the nonvolatile memory by the write data.